REMARKS

The Office action of July 3, 2003 has been received and its contents carefully noted.

Claims 1-10 are pending in the application. Claims 1 and 6 have been amended.

Claims 1 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Figures 9-11 in view of Nobutani et al. ("Nobutani") (U.S. Patent No. 5,736,981) and Hanami et al. ("Hanami") (U.S. Patent No. 6,125,432). Claims 2-6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Figures 9-11 in view of Nobutani, Hanami, and Shimizu (U.S. Patent No. 6,043,803). Claims 7-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Figures 9-11 in view of Hanami and Shizmizu. Applicants respectfully traverse these rejections, and request allowance thereof in the continuation prosecution application for the following reasons.

Substance of Examiner Interview

Applicant acknowledges with appreciation the courtesy extended to Applicant's representative by the Examiner during the interview conducted on May 6, 2004.

Applicant's representative and Examiner discussed the allowability of claim 1 in view of the cited prior art, Nobutani and Hanami. The examiner maintained the rejection of the last office action mailed March 19, 2004 for this claim based on the

view that the partial rewrite operation disclosed by Nobutani may be combined with the buffer memory access of Hanami to disclose the recited subject matter.

In response to the maintained rejection, representative agreed to amend claim 1 to distinguish the cited art where Examiner agreed that clarifying that our recited display control device does not generate or transfer a flag associated with the detected region would distinguish the cited art.

The Claims are Patentable Over the Cited References

Combination of Nobutani and Hanami is Improper

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103, the rejection must identify some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the cited references. *MPEP §§ 706.02(j), 2142.* When the motivation to combine the references is not immediately apparent, it is the duty of the examiner to explain why the combination of the references is proper. *MPEP § 2142.* Additionally, the mere fact that references can be combined does not support a proper obviousness rejection unless the desirability of the combination is also suggested in the prior art. *Id.*

Applicants strongly contend that these MPEP requirements are not met by the rejection of Claims 1-10 as the combination of the Nobutani and Hanami references is improper since there lacks any

suggestion or motivation to combine these two references. Nobutani describes a display control apparatus for a display device capable of performing a partial rewrite operation by detecting a specific rewrite pattern (a cursor pattern) and transferring a line address for the cursor before and after movement to perform the update on the display device, (see FIGs. 4, 11-13; Abstract, col. 11, lines 43-59; col. 12, lines 38-47). In contrast, Hanami does not describe a display control device, but solely describes an image processing apparatus that enables high-rate data transfer, without using a host computer, between the apparatus and an external communications device using a frame buffer memory. (see FIG. 1; col. 5, lines 66-67; col. 6, lines 8-18). Hanami solely mentions transferring image data at a high rate into the frame buffer memory as received from the external communications device, and makes no mention of transferring data from the memory to a display device using a display controller for updating the display device. Therefore, it would not be obvious to combine Nobutani and Hanami since Nobutani describes updating a display device by transferring updated image data from a memory in the display device controller to the display device which is a vastly different subject matter from Hanami's disclosure of a transferring data from an external communications device to a frame buffer of a image processing apparatus.

Nobutani is solely directed towards rewriting a cursor display on a display device using flag/data updates of the display

controller memory, while in contrast, Hanami makes completely no mention of updating a display device using a display controller and instead is directed towards an image processing device enabling high-rate image data transfer from an external communications device to a frame buffer. Simply put, Hanami does not describe a display control device but rather an image processing device for enabling high-rate image data transfer from an external device for storage in an internal memory, and Applicants strongly contend that transferring data from a display controller to a display device is vastly different from transferring data from an external communications to the frame buffer of an image processing device. Furthermore, Hanami strong teaches away from Nobutani by solely disclosing a complete rewrite operation (using block-by-block rewriting and transfer) which directly contrasts with Nobutani disclosing a partial rewrite operation for a cursor.

Therefore, due to the significant distinction in subject matter presented by these two references, it would not be obvious to combine the display device update apparatus of Nobutani with the high-rate data transfer system of Hanami.

Claims 1 and 11 are not made obvious in view of FIGs. 9-11, Nobutani, and Hanami

Claims 1 and 11 stands rejected under § 103(a) in view of FIGs. 9-11, Nobutani, and Hanami. Applicants strongly contend that these references, either alone or in combination, fail to disclose

the features recited in this claim as amended such as a write region detection means responsive to addresses accessed by the image data writing means for detecting a region including all the addresses being accessed without generating and transferring a flag associated with said detected region, wherein when the image data writing means issues a transfer command, said transfer means transfers to the display means only such data that is in the region detected by said write region detecting means.

Neither Nobutani nor Hanami disclose this patentably distinct feature of a write detection means for detecting a region including all the addresses being accessed by an image data writing means without generating and transferring a flag associated with said detected region, and wherein a transfer means transfers to a display means only such data contained within said detected region when receiving a transfer command from the image data writing means. In contrast, Nobutani solely describes a display control apparatus for a display device capable of performing a partial rewrite operation by detecting a specific rewrite pattern (a cursor pattern) and transferring a line address and associated flag information for the cursor before and after movement to perform the update on the display device. (see FIGs. 4, 11-13; Abstract, col. 11, lines 43-59; col. 12, lines 38-47).

Specifically, Nobutani detects and transfers single line addresses and must detect and transfer associated flag information of the cursor pattern using a rewrite detector/flag generator to

update the display device (FLCD) in contrast to the recited feature of detecting and transferring a region including all detected addresses using a write detection means for detecting the region including all the addresses being accessed by an image data writing means without generating and transferring a flag associated with said detected region, and a transfer means transferring to the display means only such data that is in the region detected by said write region detecting means. Particularly, Nobutani discloses that "...when a partial rewrite operation for the cursor movement is to be performed, only the address (source top line address) of the top or uppermost line of the cursor pattern before the movement is transferred to the flag set circuit...reads out these pieces of set flag information in a predetermined order and transfers the readout information to the line address generator...subsequently, only the address (destination top line address) of the top or uppermost line of the cursor pattern is transferred to the flag set circuit...set flag information is transferred to the line address generator." (see FIGs. 4, 11-13; col. 11, lines 43-59).

Furthermore, Nobutani states that "...of all the cursor line flag information transferred to the line address generator, flag information associated with the line of the source cursor pattern is preferentially transferred...for this reason, the rewrite address generator requests to the SVGA display data of a line address of flag information to be transferred next...the SVGA reads out the display data at this line address and sends it as erase data to the

FLCD." (see FIGs. 4, 11-13; col. 12, lines 38-47). Therefore, Nobutani fails to disclose the recited feature of a write detection means for detecting a region including all the addresses being accessed by an image data writing means without generating and transferring a flag associated with said detected region, and detecting and transferring the detected region to the display means as in contrast Nobutani solely detects and transfers single line addresses along with associated flag information to perform the updating of the display.

Similarly, Hanami does not disclose the recited features. In contrast, Hanami does not describe a display control device as recited, but solely describes an image process apparatus that enables high-rate data transfer, without using a host computer, between the apparatus and an external communications device using a frame buffer memory. (see FIG. 1; col. 6, lines 8-18). Hanami solely mentions transferring image data at a high rate into the frame buffer memory as received from the external communications device, and makes no mention of the recited feature of a write detection means for detecting a region including all the addresses being accessed by an image data writing means without generating and transferring a flag associated with said detected region, and detecting and transferring said detected region to a display means in response to a transfer command.

Specifically, Hanami states that "...image processing apparatus thus constructed receives bit stream data from and sends out bit

stream data to an external communications unit through the buffer memory...buffer memory stores temporarily bit stream data obtained by coding pixel data by the variable length processor included in the control unit...only the bit stream data can be transferred without relying on the host computer which enhances data transfer rate...a system including a synchronous DRAM as the frame buffer memory." (see FIG. 1; col. 5, lines 66-67; col. 6, lines 2-7, 31-32). Therefore, Hanami solely discloses an image processing apparatus for enabling high-rate transfer of image data from an external communications device to a two-bank frame buffer in contrast to the recited feature of transferring a detection region of addresses to a display means. Hanami does disclose transfer of a rectangular region of pixel data to the frame buffer memory, but again there is no mention of transferring a region of detected addresses to a display means in response to a transfer command as recited. Therefore, Hanami completely teaches away from and omits the recited feature as Hanami solely describes transferring image data from an external communications device to an internal frame buffer memory in contrast to the recited invention of transferring a region of all detected addresses from a graphics memory to a display means.

Therefore, Hanami solely discloses an image processing apparatus for transferring image data at a high rate from an external communications device to an internal frame buffer memory without any mention of transferring a region of addresses to a

display means while Nobutani solely discloses detecting and transferring single line addresses including associated flag information to a display control device for updating a display device.

Furthermore, even if the frame buffer memory of Hanami is considered part of display means 14, there is completely no mention of a rewrite operation throughout the disclosure of Hanami. Hanami still completely rewrites the entire screen of data using block-by-block (rectangular region-by-rectangular region) rewriting and transfer as disclosed in contrast to the recited feature of a transfer means transferring to the display means only such data that is in the region detected by said write region detecting means.

Thus, the combination of Hanami and Nobutani still omits the recited feature of a write detection means for detecting a region including all the addresses being accessed by an image data writing means without generating and transferring a flag associated with said detected region, transferring the detected region to a display means in response to a transfer command, and a transfer means transferring to the display means only such data that is in the region detected by said write region detecting means. Therefore, it is clear that both Nobutani and Hanami, either alone or in combination, do not disclose the recited features making the claimed invention patentably distinct and non-obvious from both references.

Claims 2-6 are not made obvious in view of FIGs. 9-11, Nobutani, Hanami, and Shimizu

Claims 2-6 stand rejected under § 103(a) in view of FIGs. 9-11, Nobutani, Hanami, and Shimizu. Applicants strongly contend that these references, either alone or in combination, fail to disclose the features recited in these claims as amended such as a write detection means for detecting a region including all the addresses being accessed by an image data writing means without generating and transferring a flag associated with said detected region, wherein when the image data writing means issues a transfer command, said transfer means transfers to the display means only such data that is in the region detected by said write region detecting means to reduce the amount of data transferred and reduce the power consumed by said display control device.

As contended above, both Nobutani and Hanami fail to disclose these recited features. Similarly, Shimizu fails to discloses these recited features as Shimizu solely discloses a liquid crystal display device capable of adjusting the dot clock signal frequency. Furthermore, Shimizu specifically states "...the screen size detecting circuit 17 detects the clocks during an effectively displayable signal period of the horizontal image signal period...the screen size detecting section 17 outputs the minimum value of the image display start positions and the maximum value of the image display end positions for one screen, to the microcomputer, 15, as

screen size data based on the detecting results." (see col. 4, lines 60-67).

Thus, Shimizu solely discloses that the start and end positions are of an effective signal area, and not the start and end positions of the area having been rewritten in contrast to the recited feature of a write detection means for detecting a region including all the addresses being accessed by an image data writing means without generating and transferring a flag associated with said detected region, and a transfer means for transferring to the display means only such data that is in the region detected by said write region detecting means. Therefore, it is clear that Shimizu does not disclose the recited features making the claimed invention patentably distinct and non-obvious from these references.

Claims 7-10 are not made obvious in view of FIGs. 9-11, Hanami, and Shimizu

Claims 7-10 stand rejected under § 103(a) in view of FIGs. 9-11, Nobutani, Hanami, and Shimizu. Applicants strongly contend that these references, either alone or in combination, fail to disclose the features recited in these claims such as determining an image data region, being less than a full display screen of image data, including said addresses being accessed without generating and transferring a flag associated with said determined region, and transferring image data within said image data region to said display device.

As contended above, Hanami fails to disclose these recited features. Similarly, Shimizu fails to discloses these recited features as Shimizu solely discloses a liquid crystal display device capable of adjusting the dot clock signal frequency. Furthermore, Shimizu solely discloses that the start and end positions for the screen size detection are of an effective signal area, and not the start and end positions of the area having been rewritten in contrast to the recited feature of determining an image data region, being less than a full display screen of image data, including said addresses being accessed without generating and transferring a flag associated with said determined region, and transferring image data within said image data region to said display device.

Therefore, it is clear that Shimizu does not disclose the recited features making the claimed invention patentably distinct and non-obvious from these references.

Conclusion

In view of the amendments and remarks submitted above, it is respectfully submitted that all of the remaining claims are allowable and a Notice of Allowance is earnestly solicited.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayments to Deposit Account No. 02-2448 for any additional fees

required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

The Examiner is invited to contact the undersigned at (703) 205-8000 to discuss the application.

Respectfully submitted,

BIRCH, STEWART, KOLASCH, & BIRCH, LLP

By Clint Dorcline 4/1035
Michael K. Mutter, Reg.#29,680

MKM/CAG:tm
1190-0498P

P.O. Box 747
Falls Church, VA 22040-0747
Phone: (703) 205-8000